Final report

1.1 Project details

Project title	The world's smallest, lightest and most efficient charger
Project identification (program abbrev. and file)	64014-0558
Name of the programme which has funded the project	EUDP
Project managing company/institution (name and address)	NPC Tech ApS, Smedeholm 13A, 1. th, 2730 Herlev
Project partners	NPC Tech ApS and DTU Electrical Engineering, Technical University of Denmark
CVR (central business register)	36052651
Date for submission	27. september 2019

1.2 Short description of project objective and results

1.2.1 English version

Based on a patent pending solution from Nordic Power Converters and the IC expertise of DTU Elektro the project partners will develop a charger technology for laptops, tablets, and mobile phones, 80% smaller, 50% less expensive, and 10% more efficient than standard power converters.

The project has developed four demonstrators, each showing improvements. Through the advancements made on the ACDC converter, the developed charger has improved both in size, cost, efficiency and PF. Two types of synchronous rectifiers (SR) were developed. SR improved the efficiency by up to 0.9%. The solutions for SR is monolithically integrable, giving lover cost and further size reductions.

The resulting demonstrators showed a possible size reduction of 68%, a cost reduction of up to 25%, and an efficiency improvement of 8%. While not fully meeting the project objectives, they still show significant improvements over current state-of-the-art.

1.2.2 Dansk version

Med udgangspunkt i en patenteret løsning fra Nordic Power Converters og DTU Elektros IC-ekspertise vil partnerne udvikle en oplader til laptops, tablets og telefoner mv., der er 80% mindre, 50% billigere og 10% mere effektiv end normale strømforsyninger.

Projektet har udviklet 4 demonstratorer, der hver især viser forbedringer. Den udviklede ACDC-oplader har forbedret både størrelsen, produktionsprisen, effektiviteten og PF. To typer synkrone ensrettere blev udviklet. Disse gav en forbedring på op 0.9% effektivitet, og er fuldt monolitisk integrerbare. Dette betyder lavere omkostninger samt mulighed for yderligere størrelses-reduktion.

De udviklede demonstratorer viser en potentiel størrelses-reduktion på 68%, sænker omkostningerne med 25% og har en total effektivitetsforbedring på 8%. Dette er ikke helt de forventede forbedringer, men er stadigvæk en væsentlig forbedring ift. State-of-the-art.

1.3 Executive summary

This project aims to make chargers that are profoundly smaller, lighter and more efficient than any chargers in the market today.

Nordic Power Converters (NPC), a spinout from the Technical University of Denmark (DTU), has developed a generally applicable technology reducing size and cost of power converters significantly while increasing efficiency: Size and weight are down 80%, cost down 50%, and efficiency increased from the typical 75- 85% range of market products to >90%. All done without compromising quality or durability. Downsizing parts of the invention to chip-level is done in close cooperation with DTU Elektro, who are experts in IC- design.

Around 500 million laptop and tablet chargers along with almost 2 billion mobile phones are sold every year. The reductions in cost and size allow for new applications and new designs of existing applications, rendering the patented method the potential to revolutionize the +DKK 110 billion market for power supplies.

This project is needed to demonstrate the technology's superior qualities to manufacturers of power converters. The project addresses a series of technical and commercial objectives that need to be accomplished to do so.

In the project the initial demonstrator quickly showed improvement over the current state-of-the-art solutions reducing the cost by 20%, and size by 61%. It also provided improvements of both PF and efficiency compared to state-of-the art. Simultaneously it showed the requirement for synchronous rectification inside the ACDC converter.

For this purpose, DTU has developed two integrated circuits for synchronous rectification. These ICs used phase- and delay-locked-loops, technologies known from other fields, in the new setting of power electronics. This provides novel solutions for improving the efficiency over the passive rectifier. It further improved the efficiency of the converter by up to 0.9% and can be expected to be doubled in a full implementation. The developed solutions are fully integrable, meaning that the path for a monolithically integrated synchronous rectifier is now paved. This is both a smaller and cheaper solution for large scale market, such as the charger market.

A switched capacitor solution was implemented in two of the demonstrators. While improving the efficiency especially at low voltage, this solution was also expensive, primarily due to the requirement for bleeding edge transistor technology in GaN devices.

The project puts power converters on the roadmap towards pure chip design. In doing so it also puts the converters into the regime of Moore's Law, where it can be expected that over time power converters will go from consisting of many components to still fewer components until some converters ultimately are embedded in a single chip. At which point in time it is likely that there will only be very few power converter manufacturers left in the world.

The combination of the ACDC converter together with the novel developed synchronous rectifiers show a potential for reducing the size of the charger by 68%, the cost by 25% and an efficiency improvement of 8%. This is substantial improvements over the current state-of-the-art.

1.4 Project objectives

1.4.1 Project objectives, challenges and risks

The main project objectives (OB1-3) were as described in section 1.2 to develop a charger for laptops, tablets, and mobile phones offering:

- OB1. 80% size reduction
- OB2. 50% cost reduction, and
- OB3. 10% increase in efficiency

This charger should be developed to a maturity level where it could be demonstrated to leading manufacturers.

The main technical challenges (CA1-3) to be addressed to reach this goal was:

CA1. Optimization of the mains rectifier and associated losses
CA2. Development of an efficient high frequency AC-DC power stage
CA3. Development of a synchronous rectifier for the AC-DC power stage

From the beginning of the project the main risks (RI1-4) within the project were identified to be:

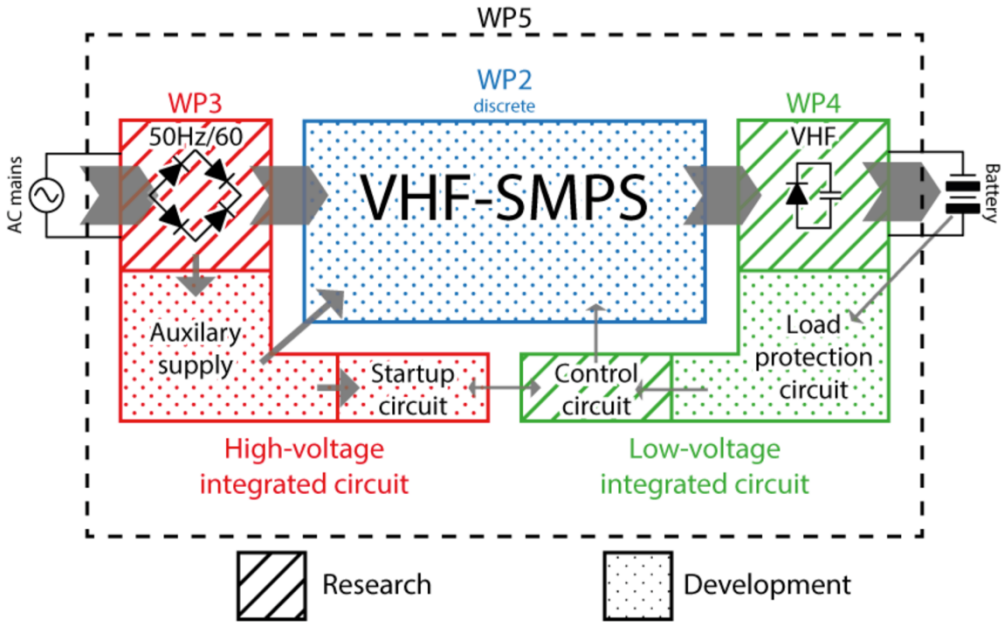
RI1. Adapting the technology from LED bulbs to charger
RI2. Increasing the power range while keeping the size small
RI3. Completing six tape-outs and their associated costs
RI4. Thermal management of the ICs

Another real risk was that some other companies would develop another solution faster.

One of the planned mitigations was to develop the charger with partial ICs and standard discrete components, if the challenges with getting all the ICs through turnout to be big. It was noted that this would have an impact on reduction of size and cost, but not to an extent that will eradicate the benefits fully.

1.4.2 Project plan

The project was planned to be carried out in 5 work packages as illustrated and listed below.



Work packages	
WP1 System Engineering	System level portioning of the DC-DC converter is essential to achieve tight integration. WP1 will identify the specification for the system.
WP2 Discrete design	First year of the project all the components needed for a complete working prototype will be designed and implemented. In the rest of the project the focus will be to optimize the power stage (PS) to achieve high efficiency and power density.
WP3 High voltage (HV) IC	As the HV IC has to interface to an AC mains a HV process is needed for this. In this IC the rectifier interfacing to the AC wall outlet will be implemented and optimized This IC will also contain start-up and protection circuitry needed.

WP4 Low voltage IC	The VHF rectifier and all the circuitry needed for the regulation will be implemented in this IC including circuitry that monitors and protects the load.
WP5 Demonstrator	4 demonstrators will be implemented during the project to test compatibility of the blocks and the overall system. The demonstrators will be used as show case for potential partners.
WP6 Project management	This work package will coordinate the work packages, do the reporting and coordinate changes if necessary. Workshops will be arranged every 3rd month.
Research Milestones	
R1 Active power line rectification	Today the powerline rectifier is one of the largest components and thus the size of this component will be minimized.
R2 Integrated active VHF rectifier	The active VHF rectifier must be optimized for high frequency operation to ensure low losses. This requires detailed optimization of the parasitics in the IC process.
Technical Milestones	
T1 PS prototype	Fully functional PS designed to the input and output specification defined in C1.
T2 Discrete protection, start-up and auxiliary supply circuit	These circuits will be used for the first demonstrators and serve as a starting point for the IC design.
T3 Discrete control loop	The control circuit will be designed to insure proper charging of the battery.
T4 IC TO 1	Tape-out (TO) 1 will implement the most critical blocks and some test structures in order to characterize and validate the selected processes.
T5 Optimized PS	The optimized PS will have higher efficiency and power density than the first prototype. Galvanic isolation according to safety standards will be in place.
T6 IC TO 2	TO 2 will implement the first version of the circuitry needed for the HV and LV parts based on the finding from T4.
T7 90% efficient PS	The 3rd version of the PS is expected to achieve an efficiency of at least 90% demonstrating that highly efficient chargers can be achieved with NPCs technology.
T8 IC TO 3	TO 3 will implement the final solution. Based on the findings from T6 and the first prototype with optimized integrated blocks.
T9 High density PS	At the end of the project a charger with a power density higher than current state-of-the art (~2W/cm3) will be implemented, hence 3W/cm3 is targeted.
Commercial milestones	
C1 System	Initially the system specifications and the interface between the

specifications defined	blocks will be defined.
C2 1st prototype	This demonstrator will be the first circuit showing the fully functional charger and serve as a bench mark for the efficiency and size of the future demonstrators.
C3 IC process tested	The first important milestone in the IC track will be to identify processes for implementation of the ICs.
C4 First prototype with integrated blocks	The blocks from WP2-4 are connected and the compatibility of the output from the WPs is demonstrated.
C5 Roadshow	When the 2nd demonstrator with integrated blocks is ready a roadshow to major power converter manufacturers and buyers will be carried out in order to find partners for the demonstration phase.
C6 The world's smallest, lightest and most efficient charger	At the end of the project a fully working demonstrator will showcase the world's smallest, lightest and most efficient charger.

1.4.3 Project execution

One of the first activities in the project, was to have a meeting with Sten Carlsen who was a member of the who sets the specifications for the new USB-C and USB 3.1 standards. Following that it was quickly decided to set the specifications for the project to meet these standards (C1 was thereby meet). This put increased requirements on the charger, but was not expected to influence the overall project plan and objectives.

The development of the first power stage was more challenging than expected, even though that was identified as one of the biggest challenges (CA2) and addressed to of the biggest risks (RI1+2). This led to delays in T1, but the results were better than expected. Especially for the efficiency which was one of the main objectives for the project (OB3).

It also took longer than expected to find the right PhD candidates to carry out the IC design. Developing the needed IC in time was already identified as one of the big risks of the project (RI3) and the project plan had to be revised, the milestones and duration of the project where however kept.

At the time of the third annual report (41 months in to the project with a total duration of 56 months), the project was still developing in accordance with the revised plan. The project had also reached a major milestone by completing C2.

At the same time, the project had however experienced difficulties with the selected IC process. Due to unforeseen difficulties, the IC process used for the initial synchronous rectifier was cancelled by the manufacturing company, resulting in a change of IC process. This meant a complete redesign of the synchronous rectifier, as well as no possible reuse of previously designed critical blocks. On top of that DTU experienced some challenges with the resources allocated for the project as one of the PhD students had paternity leave twice, the other decided to terminate his studies and one of the two senior researchers where long term ill.

Due to these delays and resource challenges, it was decided to apply for an extension of the project. At the same time it was decided to go for a discrete implementation of the mains rectifier, instead of the integrated active rectifier (CA3) which the terminated PhD student was responsible for. The extension and a new project plan with focus on bringing the technical results into demonstrators was accepted.

The demonstrators were:

Demonstrators	
Demo 0	Previously referred to as milestone C2.
Demo A	Complete USB-C charger with NPC HF power stage, synchronous rectification and USB communication.
Demo B	Demonstration of a switch-cap circuit to control the three output voltages (5, 12 and 20V).
Demo C	Demonstration of the latest generation of the main power stage with synchronous rectification and the third generation IC, a switch capacitor output and USB-C communication.

Both Demo A, B and C was completed and the results are described in the next section.

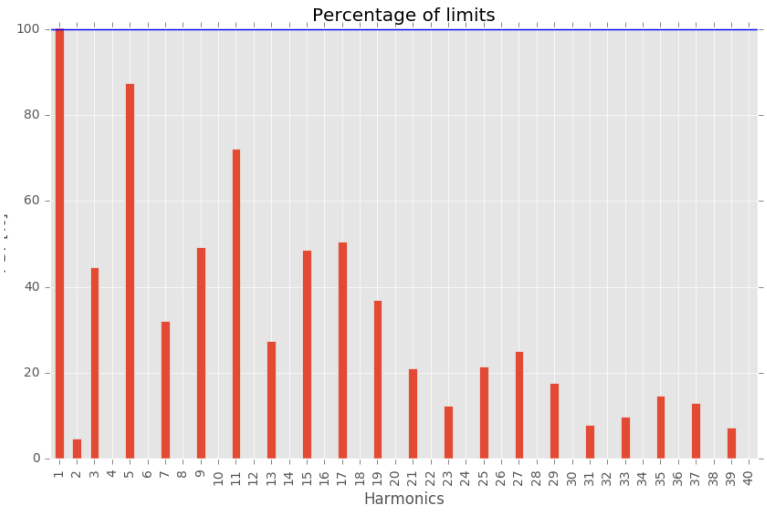
1.5 Project results and dissemination of results

1.5.1 Demo 0

The first demo that was ready (Demo 0 or C2 from the original plan) was a bit delayed, but the results surpassed the expectations. The main results were:

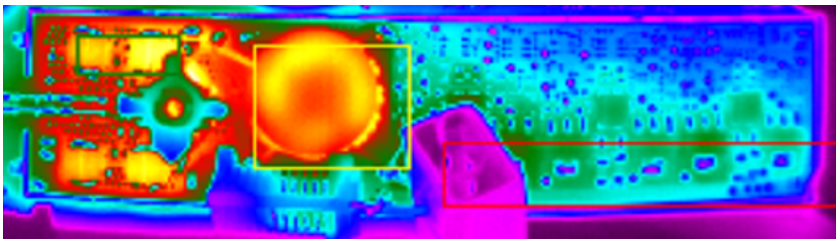
Input	Output	Efficiency	PF / THD	Size (box)
230 V / 50 Hz	20 V / 2.3 A (45W)	>83%	0.98 / 16.5%	13 x 2.5 x 1.2 cm

These results significantly surpass the expectations, especially on power factor and harmonic distortion (THD). There are no formal requirements for these for products below 75 W, but expectation is that they will come and the prototype has a performance that is better than the requirements for 75 W products. For US/UL the requirement is a PF >0.9 and for EU/CE the requirement is for the individual harmonics, also here the prototype is way below the limits as seen in the graph below.



The size was also better than expected for the first prototype without the ICs. The box volume was 39 cm^3. Apple is known for their compact chargers and at the time their 60 W took up 102 cm^3. Since then competitors have appeared with chargers around 45/50 W and volumes around 50 cm^3. The commercial chargers include plug and casing, which is not the case for the prototype. It is however possible to pack the components on the prototype closer in a final product and the IC should help to reduce the size significantly. This was hence a great step towards meeting the objectives of the project.

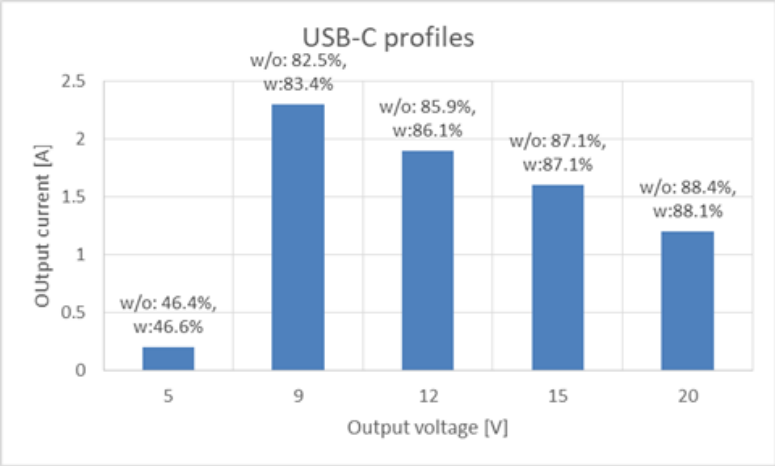
The first prototype was below the target for efficiency, with an efficiency of 83% compared to the target of 90%. The lower efficiency also led to a limitation of 45 W due to the thermal design. A thermal image of the prototype is shown below.



The picture shows that 5 components were getting hot and thereby were the main causes of losses. Four of these components are the diodes which would be replaced by more efficient MOSFETs when the synchronous rectifier was ready. It was hence expected that the synchronous rectifier would enable the efficiency needed to meet OB3. The efficiency was later increased to 87% without the synchronous rectifier.

1.5.2 Demo A

The circuit was able to deliver all the voltages required by the USB-C standard (5, 9, 12, 15 and 20 V). It was also clear to see that the synchronous rectifier improved the performance at low output voltages. In the measurements below only one of the diode pairs was replaced by the synchronous rectifier, it was hence expected that twice the improvement could be achieved by replacing both. The thermal images also clearly showed reduced temperatures.



The circuit was not able to deliver the planned current at 5 V. This was due to the timing in the synchronous rectifier and was expected to be improved in the next IC.

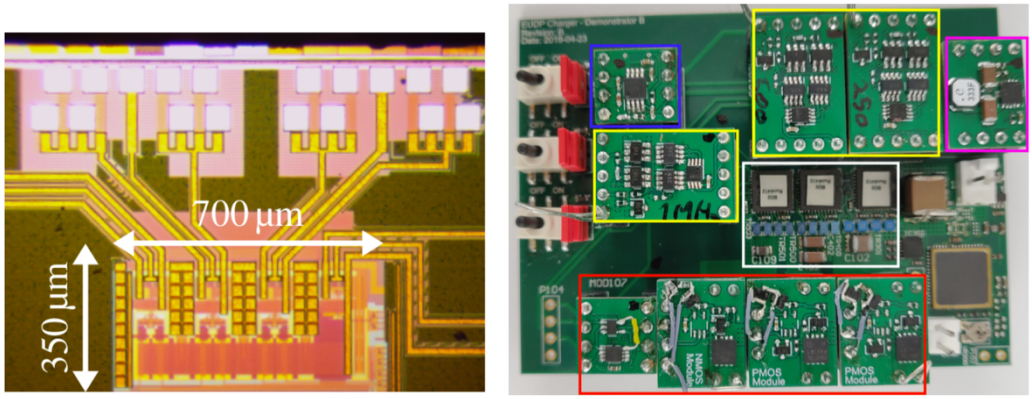
It was another important step for the project to reach a full system demonstrator with a performance close to the specifications. Having a functional synchronous rectifier was also an important research result.

1.5.3 Demo B

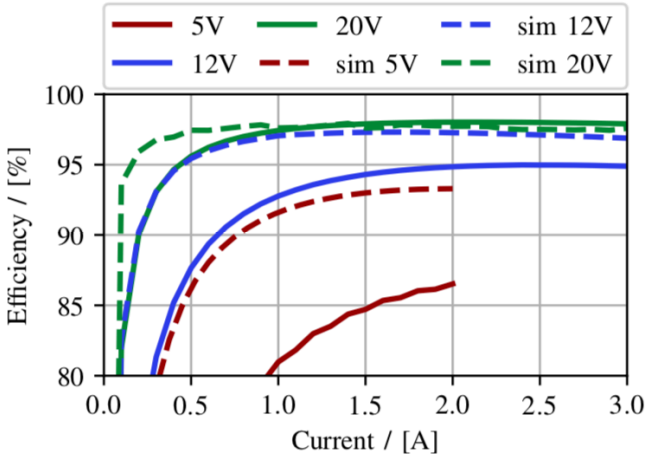
As the losses in the resonant ACDC converter are very dependent on the output voltage, a solution using a switch capacitor circuit to convert from 42.5 V to the 5-20 V output was developed.

An ASIC containing the necessary level shifters and gate drivers are was taped out. The ASIC was then implemented on a PCB with 3 stages – a voltage division of 2:1, 4:1, and 8:1. This would allow to narrow the output voltage range for the RF-SMPS, and efficiently down convert the output voltage.

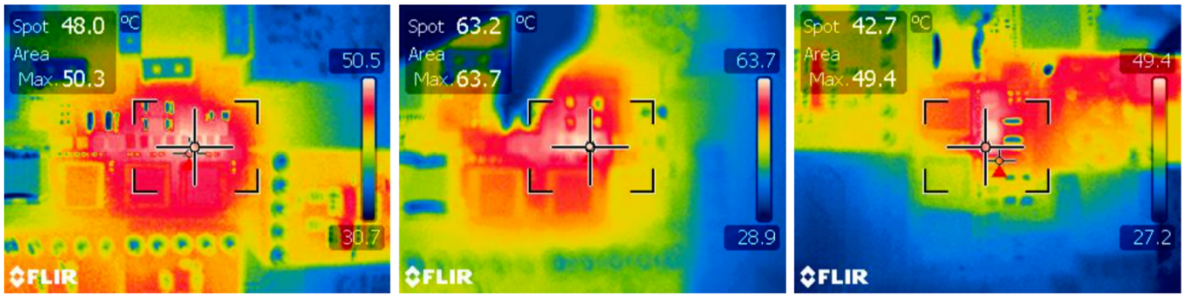
Below the die photograph of the ASIC is shown, next to the PCB for the prototype.



The efficiency is shown in the graph below. Aside from the 5 V, both the 12 and 20 V output have peak efficiencies above 95 %, which would allow efficiently down conversion of the output voltages. All of the external circuitry shown in both blue and yellow above can be integrated monolithically on a die.



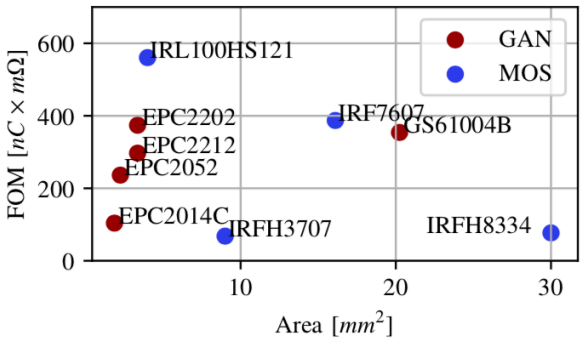
Thermally they are shown to perform as well. Below the thermal photographs are shown, at 10 W, 36 W and 60 W respectively.



The above results are submitted for the 4th IEEE International Future Energy Electronics Conference (IFEEC 2019).

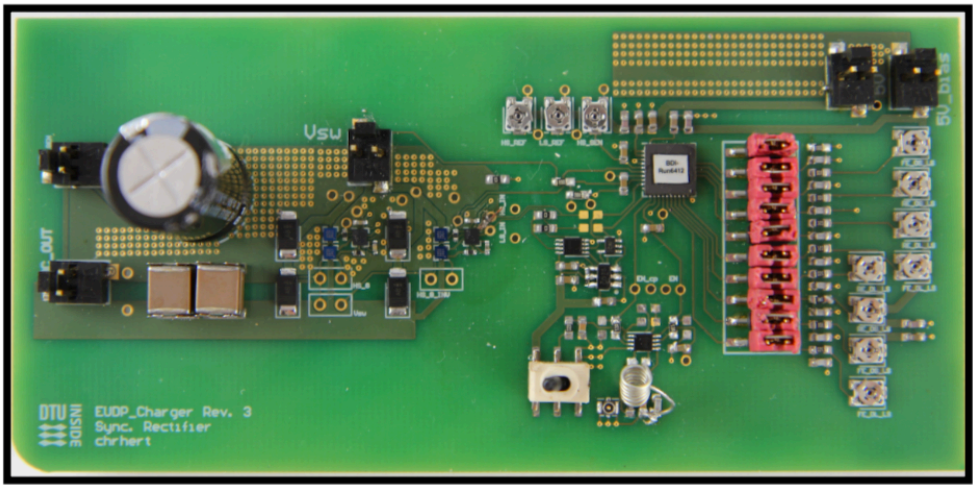
Demonstrator B showed that a switch capacitor circuit could be used to generate the 5-20 V needed at the output. The peak efficiency was 98% and the efficiency dropped 3% when the voltage was reduced from 20 to 12 V and additional 8.5% when the voltage was reduced further to 5 V. The efficiency increase in the ACDC converter was approx. 2.5%. The gain was hence small for 20 V output and also for 12 V where the drop was approx. 2% for both solutions. The improvement was however big for 5 V where the resonant converter had an efficiency drop of approx. 40%. The switch capacitor circuit did hence not show significant improvements at 20 or 12 V output, but a very big improvement at the lowest voltage.

The switched capacitor circuit was implemented with GaN devices, as these have state-of-the-art performance. In relation to the switched capacitor design, a study was conducted on available FETs. In the graph below, the GaNFETs are compared to state-of-the-art MOSFETs. The best performance is achieved with as low a FOM as possible, and as can be seen, in terms of area vs FOM, the best performance is achieved with GaN. However, at the current market, the price of GaN is much higher, and would impact the cost significantly.

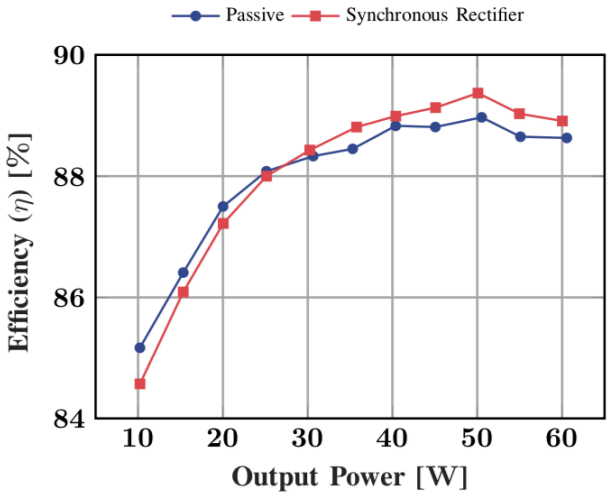


1.5.4 Demo C

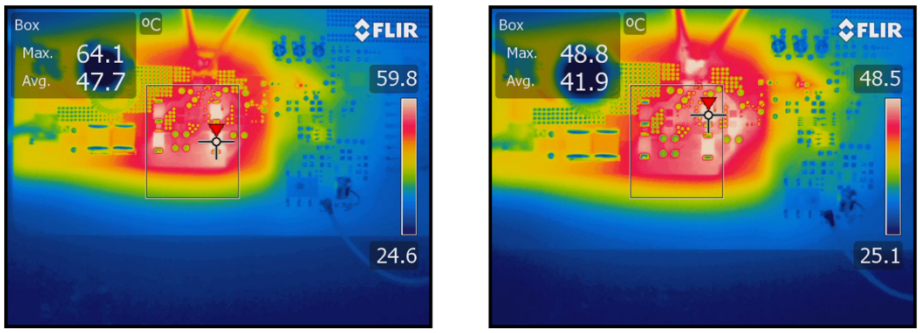
The last demonstrator intended to implement a new synchronous rectifier, together with results from Demo B. The new synchronous rectifier was designed with the experienced gained from SR in Demo A and designed to synchronize the rectifier faster and allow for higher efficiency all together. Demo C should further include the switched capacitor circuit from Demo B. Below a photo of the PCB designed for the synchronous rectifier is shown.



At an output voltage of 42.5 V of the synchronous rectifier, the diode in the passive rectifier performs much better than at lower output voltages. Even so, the SR still improved the efficiency of the designed converter, by 0.4%, shown in the graph below.



Along with the improvement in efficiency, the thermal properties were improved. Below the thermal pictures of the setup is shown.



(a) Thermal Picture of with the SR turned off.

(b) Thermal Picture of the SR turned on.

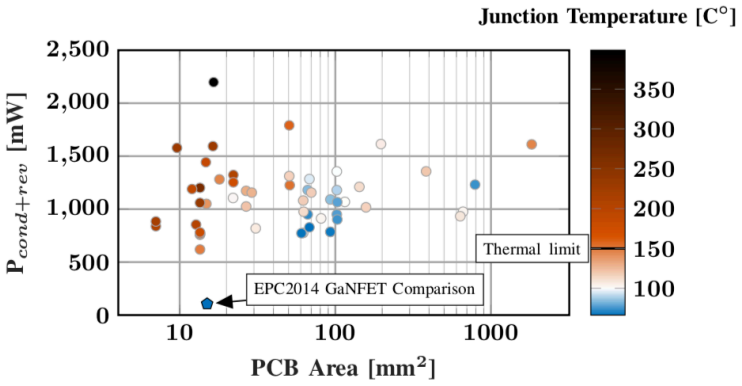
The temperature is seen to not exceed 50 ºC, under 50 W load, improving the thermal specifications, and allowing to pack the converter smaller and closer together.

Several challenges however meant, that a full Demo C was never implemented. During the development of Demo C, the IC designed showed to be working as planned, however, implementation in a power converter proved more challenging. Among these, were the initial stabilization of the frequency in the resonant converter, the asymmetry in the passive full bridge rectifier, and the changing frequency under ACDC conversion. Some of these challenges could be solved by implementing another IC, controlling the two half-bridge asymmetrically, which would both improve the efficiency, and thermal properties of the converter. Due to time issues, these developments were not realized.

1.5.5 Synchronous rectifier

The synchronous rectifier is the strongest research results from this project, it is therefore described in more details in the following subsections.

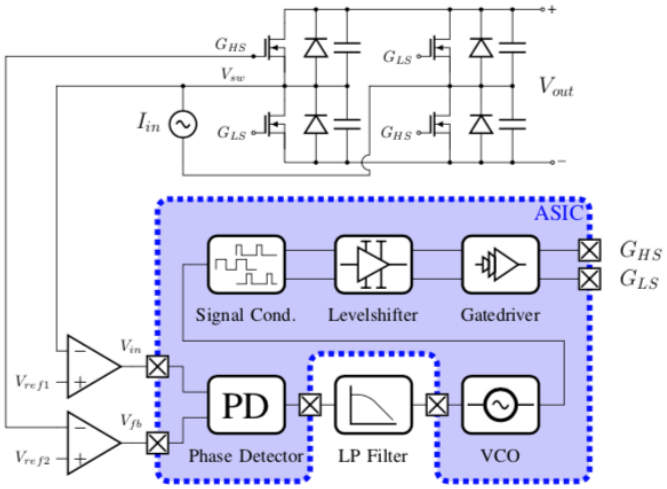
Through this work, it quickly became apparent that the need for another method of rectifying the high frequency current from NPCs inverter was quintessential to achieve both the efficiency and thermal capabilities needed for a power converter of the desired size. The current solution using diodes are inherently very lossy. In the figure below we show the result of a study, estimating the losses and temperatures of 70 diodes in a resonant power converter, at an output of 20 V @ 60 W. The main take-away from this figure, is that either the diodes take up a large amount of area in the designed converter, or otherwise they heat up above their thermal limit.



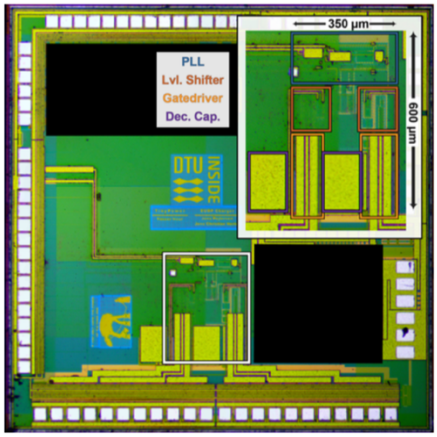
In the figure, the EPC GaNFET EPC2014, one of the current state-of-the-art switches in this power level is shown for comparison. It outperforms the diodes, in both area, power loss, and thus temperature. It was necessary to design and implement a synchronous rectifier (SR), capable of interleaving the diodes, improving both the efficiency, thermal capabilities and reducing the required areas. We have in this project developed two synchronous rectifiers, one based on a Phase-Locked Loop, and another on a Delay-Locked Loop. Both circuits known from other technical fields, but rarely employed in the field of power electronics.

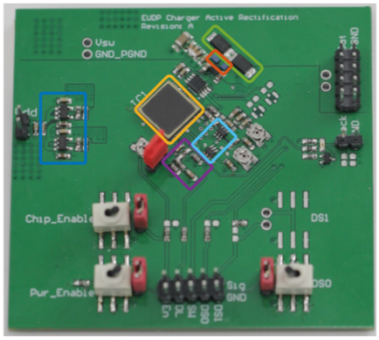
1.5.5.1 Phase-Locked Loop Synchronous Rectifier (PLL-SR)

The first SR was designed using a Phase-Locked Loop (PLL) to achieve the correct timing of gate signals. The PLL is a well-known technology known from the communication field. It is used to synchronize the phase of two signals, through negative feedback. In the figure below the principal block diagram of the SR is shown.



In order to verify the topology, the contents of the blue box was integrated on an Application Specific Integrated Circuit (ASIC). This was taped out in a High Voltage 0.18 µm CMOS process. A picture of the integrated circuits die is shown below.



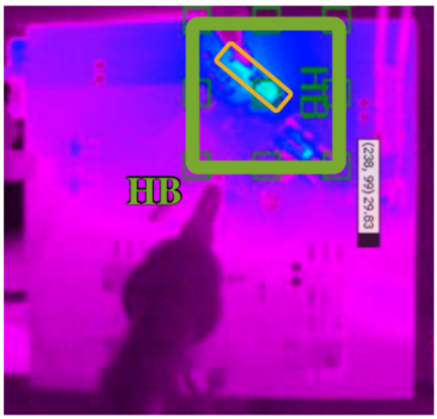


PMEG3030 Diodes | EPC2014 GaNFETs | ASIC

Loop Filter | Comparators | ASIC Power Supplies

This ASIC was implemented in a burst mode regulated RF-SMPS for the 5-20 V USB-C compliant output profile, and showed improvements in both thermal capabilities and efficiency. The PCB with the prototype is shown above, next to the die photo.

In the thermal pictures shown below, two thermal photographs are shown. The picture shows the same PCB as the picture above. The diodes of the half-bridge are shown, and without the synchronous rectification, they can be seen to heat up significantly. The implemented PCB is one half of a full bridge rectifier.

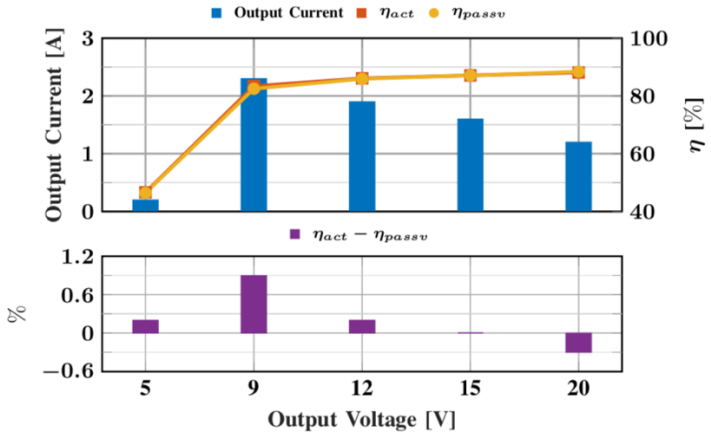


(a) Thermal picture of Passive Half-Bridge

(b) Thermal picture of Active Half-Bridge

PMEG3030 Diodes

The efficiency improvement was measured and shown below. As the implementation was one half of a full bridge rectifier, the expected efficiency improvement can be doubled. The efficiency can be seen to decrease in the 20 V output mode. This is caused by the sensing of the required gate signals. As the sensing circuits is static, the change in output voltage causes a slight timing mismatch in the switching of the synchronous power transistor. This mismatch increases the losses slightly. However, this can be fixed with a different sensing network, that would eliminate the change due to output voltage.



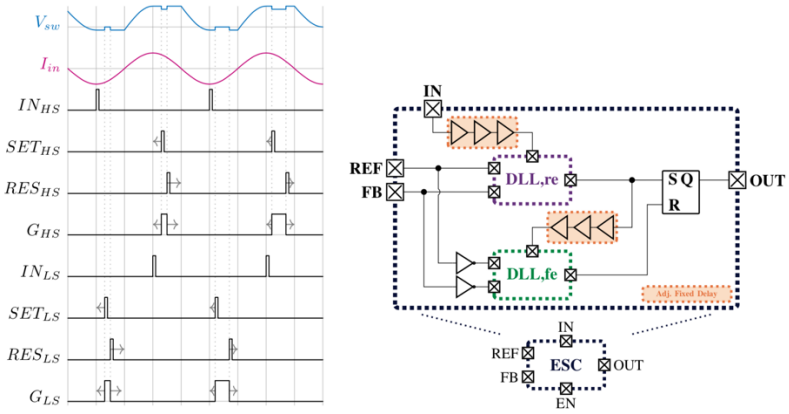
The efficiency improvement is 0.9%-points at an output of 9 V. The expected efficiency improvement is thus 1.8%-points at 9 V.

One of the largest challenges with the PLL-SR was however, that the PLL needs a certain amount of time, before synchronization is achieved. This reduces the percentage of time where the PLL-SR can interleave the diodes. As the designed SMPSs are all regulated through burst mode regulation, meaning that they are toggled on/off, the PLL would have to synchronize every time the SMPS is turned on. This limits the possible improvement in efficiency. This was addressed in the second SR designed.

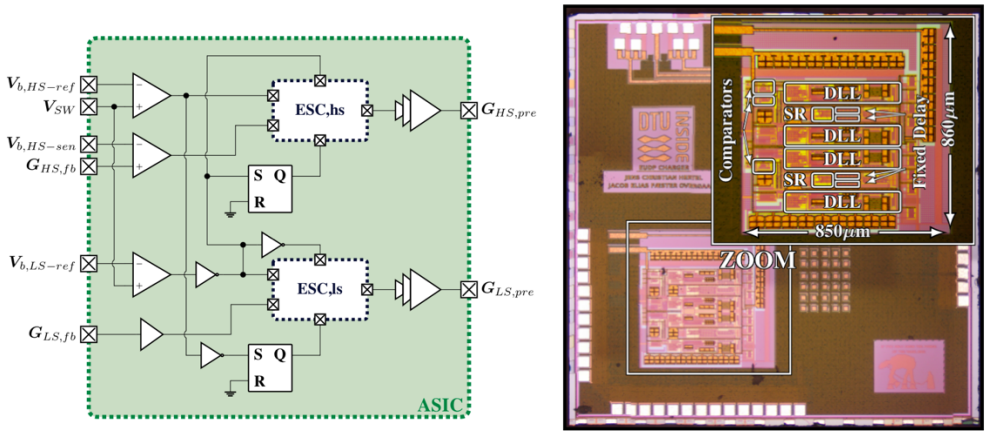
The above results are presented in an accepted, but not yet public, journal paper in the Journal of Emerging and Selected Topics in Power Electronics.

1.5.5.2 Delay-Locked Loop Synchronous Rectifier (DLL-SR)

To address the start-up problem with the synchronization, a second synchronous rectifier was designed. This utilized the Delay-Locked Loop (DLL), which is a circuit similar to the PLL. In this an ASIC was designed, intended to operate as fast as possible within a bursted on. Below the block diagram of the designed solution is presented.

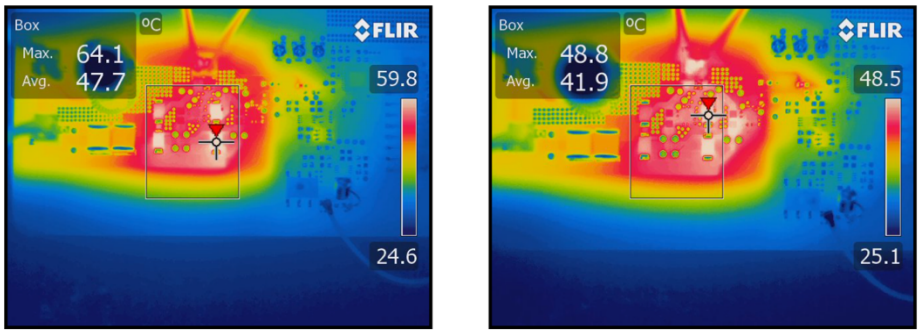


While the PLL needs time to synchronize, the proposed solution of Edge-Synchronization-Circuit (ESC) allows the SR to interleave the diodes from the first cycle. The DLL-SR will optimize the interleaving of the diodes throughout the burst on toggle. An ASIC containing two ESC was taped-out. The full block diagram is shown below, next to a die photograph.



The second synchronous rectifier was implemented in a burst mode regulated RF-SMPS outputting 42.5 V, intended for an intermediary converter, inside a USB-C compliant charger.

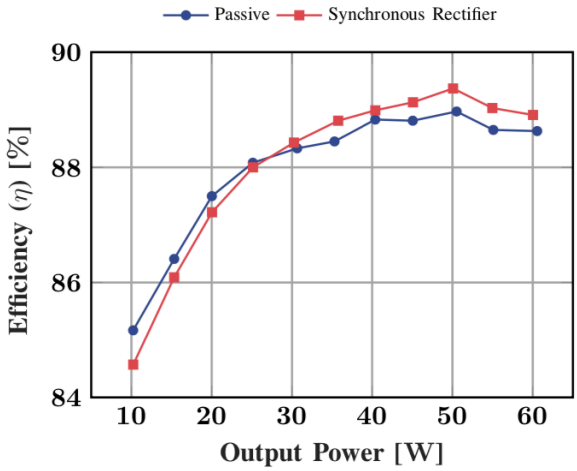
The DLL-SR showed an improvement in both thermal and efficiency as expected. The diodes drops from 64 ºC to 48.8 ºC, and the other circuitry is all below 50 ºC in the DLL-SR, significantly improving the thermal capabilities.



(a) Thermal Picture of with the SR turned off.

(b) Thermal Picture of the SR turned on.

Below the measured efficiency improvement is shown. The peak efficiency improvement is 0.4%-points. While this is slightly less than the PLL-SR, the DLL-SR is operating with an output voltage of 42.5 V. The diode losses are related to its forward voltage drop, and the proportional loss is thus much higher at lower output voltages.



One large advantage of the proposed solutions is that they work through negative feedback and are independent of the switching frequency of the resonant power converters.

The biggest advantage of both of the presented SRs are that they are fully applicable for monolithic integration, i.e. where everything is manufactured on the same die. This type of production is much cheaper in large scale production, such as a in a charger market. The future aspects for the SR are thus great.

1.5.6 Objectives

The three demonstrators are compared in the table below and compared to the objectives of the project itself further down. All though a final demonstrator was not built, the size is estimated from the final developed solution.

Result summary	η @ 5 V	η @ 12 V	η @ 20 V	Size	Cost index
Apple 60 W charger				102 cm^3	100
Demo 0			83-87%	39 cm^3	80
Demo A	46.6%	86.1%	88.1%	33-39 cm^3	75-105[1]
Demo B	75.6%	84.8%	86.8%	43 cm^3	135
Demo C	73.2%[2]	84.4%[2]	87.3%[2]	37-43 cm^3	130-160[1]

[1] The implemented synchronous rectifier is still based on several discrete components, which increase the cost. With further development these components can be fully integrated and the cost will thereby be reduced significantly.
[2] Measured with 325 V_{DC} as input due to timing issues between the burst-mode operation in the ACDC and the timing in the synchronous rectifier. These issues can easily be solved in a new iteration, but no time was left for this.

The demonstrators all provided very promising results. The solution in Demo B & C implemented a switched capacitor circuit. As can be seen, the efficiency improvement was significant at low output voltages. However, the size and cost of this solution, is larger than for both Demo 0 and Demo A. The primary influence is the GaN solution chosen for the switched capacitor. Overall, the best performance in terms of cost and size was achieved by implementing the synchronous rectifier. As the research provides a clear path towards monolithic integration of the synchronous rectifier, an overall size reduction of 68% is possible. Further the monolithic integration, being cheaper in full scale production enables a cost reduction of 25%. Efficiency was improved by 8%, only a few percentage points from the objectives. While the results are not meeting the objectives, they still provide improvement from the state-of-the-art.

Objectives vs results	Objective	Result
Size reduction (OB1)	80%	68%
Cost reduction (OB2)	50%	25%
Efficiency increase (OB3)	10%-points	8%-points

1.5.7 Dissemination

1.5.7.1 Papers

The PLL-SR was presented in Journal of Emerging and Selected Topics, selected for publication in 2019. This has been published online - DOI 10.1109/JESTPE.2019.2945542. The presented Switched Capacitor Power supply was submitted to the 4th IEEE International Future Energy Electronics Conference (IFEEC 2019).

The DLL-SR has been written for a future submission for a journal paper.

The research in this project has resulted in 1 additional journal paper, and 6 leading conference papers already published. Below the titles of the publications are given, as well a brief description of their content.

1.5.7.1.1 Very High Frequency Two-Port Characterization of Transistors

Conference contribution at the 5th International Workshop on Power Supply-On-Chip, 2016

This work detailed a method for analysing and characterization of on-chip transistors, necessary when designing High Frequency resonant power converters.

1.5.7.1.2 Integrated Very High Frequency Switch Mode Power Supplies: Design Considerations

IEEE Journal of Emerging and Selected Topics in Power Electronics, volume 6, issue 2, 2018

This work details the design of a Class E converter for a monolithic converter. The worked intended to implement self-oscillating gate drives, however found that the current state of the art technology is not sufficient.

1.5.7.1.3 Resonant Full-Bridge Synchronous Rectifier Utilizing 15 V GaN Transistors for Wireless Power Transfer Applications Following AirFuel Standard Operating at 6.78 MHz

Conference contribution at 2018 IEEE Applied Power Electronics Conference and Exposition (APEC)

This work detailed the design of a discretely designed synchronous rectifier for a wireless power transfer application. This work led to the second designed DLL-SR.

1.5.7.1.4 Low Jitter Voltage Controlled Oscillator and Gatedriver for VHF Switch Mode Power Supplies

Conference contribution at 2018 20th European Conference on Power Electronics and Applications (EPE'18 ECCE Europe)

This work detailed the oscillator design used for the PLL-SR, and presented a new simulation method for evaluating jitter in a SMPS.

1.5.7.1.5 Application Specific Integrated Gate-Drive Circuit for Driving Self-Oscillating GaN & Logic Level Power Transistors

Conference contribution at 2018 IEEE Nordic Circuits and Systems Conference (NORCAS): NORCHIP and International Symposium of System-on-Chip (SoC)

This work details the ASIC intended to precisely drive a self-oscillating transistor.

1.5.7.1.6 Using Time-Based Control Techniques for Active Rectification

Conference contribution at the 6th International Workshop on Power Supply-On-Chip, 2016

This work details the control aspects of the two presented PLL-SR and DLL-SRs respectively.

1.5.7.1.7 Time Based Control for Power Factor Corrections

Conference contribution at 2019 IEEE Nordic Circuits and Systems Conference (NORCAS): NORCHIP and International Symposium of System-on-Chip (SoC)

This work sparked from the work done on DLLs and PLLs in this project. The idea was to use elements from the DLLs and PLLs to generate control signals in the time domain, to achieve PF in a boost converter.

1.5.7.2 Patents

EP3419157A1: Power converter assembly comprising parasitic inductance balancing between multiple inverter stages

EP3539205A1: A resonant power converter

WO2018134308A1: Resonant power converter comprising ripple suppression circuit

1.5.7.3 Other

A PhD thesis, student seminars at DTU, supervision of 3 master projects, 1 master of honors student (JEFO), and several special courses for students.

1.5.8 Exploitation

Some of the results of demonstrator B have already been used in commercial products. Several thousand units have been shipped so far and many more are already ordered for the coming years. The total export value of the orders received to date corresponds to more than €500.000. It has however required significant additional investments outside of this project to reach this stage.

1.6 Utilization of project results

The competition on the charger market have increased during the course of this project. Several companies have put new smaller chargers on the market, most with limited success. The volumes in this market is very high as the solutions are very standardized and the price pressure is huge.

Very few customers are willing to pay additional for a smaller charger. Few people even notice the charger in the process of buying a laptop or a phone, it is just an accessory that follows. Another option is aftersales of additional charger is existing devices on the market, but this again is a very competitive market where big volumes are needed to get economics of scale and be competitive.

Fortunately, the results achieved in the project is a general platform for power converters, which can be applied widely. The results from demo B have already been used in commercial products for LED lighting and further products are expected to be launched towards the end of 2019 and in 2020. The results are used in combination with the foreground and sideground IP from NPC, so it is difficult to separate exactly how much revenue and how many employees are the result of this project, but the combined IP is expected to generate a revenue of approx. DKK 10M in 2020 and tens of that within the coming 5 years. This currently keeps approx. 10 full time employees employed and this number is expected to grow 2-3 times in the coming 5 years.

The results and knowledge developed in particularly the synchronous rectifier for a resonant power converter, provides a very clear path towards the monolithic integration of a synchronous rectifier. DTU is continuing to work along this path, which would be a giant leap towards smaller, and more efficient chargers.

1.7 Project conclusion and perspective

The project has achieved very promising results, especially for the ACDC converter as well as the identified critical synchronous rectifier. This has been achieved, even though the resources have been challenged by several elements, as already discussed.

For the ACDC converter, the developed prototypes showed improvements in both PF, size and cost over the state-of-the-art. There is currently no PF requirement to a commercial charger, but it is expected to be implemented soon, putting NPC at the forefront of the market. The results of the ACDC converter have already been used in commercial products.

The research results for the two synchronous rectifiers show large improvements on low voltage rectifier inside the ACDC converter. The developed technologies use well known circuits from other technological fields, which mean that they are market mature. In this project we have shown them working in the field of power electronics, and as they are fully monolithically integrable, a natural next step is to develop a synchronous rectifier that is fully integrated.

The promising results are also reflected in the 3 patents as well as 8 publications in leading conferences and journals as well as one upcoming journal publication.

The research in this project has lead to a size reduction of 68%, cost reduction of 25% and an 8%-efficiency improvement. While not fully meeting the full objectives of the research project, it still provides substantial state-of-the-art improvements and will be the subject at future projects at DTU.

Looking forward, the developed technologies from this project are both scalable and cheap. This is important in the further reduction of size and cost of a charger. The synchronous rectifier is the natural next development, where a fully integrable solution is within grasps.

Annex

Relevant links